THE DESIGN AND EVALUATION OF A PRESET, ALARMING, ELECTRONIC DOSIMETER

A Thesis

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by
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to

LIBBY

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Last but not least, Libby, my wife, who could not see the dining table for weeks at a time because of the electronic parts and books stacked precariously on every available spot.

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ABSTRACT

A major problem encountered in obtaining a successful radiograph is the determination of correct exposure dose to the imaging system. One approach to solving this problem is the development of an integrating system to indicate the correct exposure dose. An instrument to accomplish this purpose, and designed to meet practical criteria for field radiography, was constructed. Solid-state circuitry, using CMOS integrated circuit technology, was adopted for minimum power drain and compatibility with the response time of a Geiger-Muller detector. The constructed prototype instrument included LED display. In addition to the preset exposure function, the prototype instrument included a rate meter function, a scaler function, and the capability of expansion to multipoint area monitoring. The prototype instrument was found to operate as expected at low radiation dose rates. Modification of the prototype instrument for development into a field-testable instrument is described and would be based on a modular construction concept, and would include an analog readout to compliment the LED display.

CHAPTER ONE

INTRODUCTION

Radiography is one of the oldest nondestructive testing (NDT) techniques in use today. It is also one of the NDT methods enjoying widespread use and acceptance. The output of the radiography process is a visual image of the physical system under test. An imaging system (usually film) converts radiation impinging on the system detector (silver halide crystals) into a useful visual form. Radiation, produced by machine or radioisotopic sources, is attenuated by passing through the physical system under test before interacting with the detector. Changes in density, thickness, or atomic number may be detected by this NDT technique. In general, radiography refers to the technique regardless of the source type unless otherwise specified.

To produce an acceptable radiograph, the radiographer must have a knowledge of the material tested, the imaging system specifications, the source intensity, and certain geometry factors. Once all of these factors are determined it is possible to ascertain exposure time. However, these variables may not be known with a high degree of certainty. These uncertainties require the use of excessive numbers of radiographs to insure acceptable image quality.

To reduce the impact of uncertainties on the radiographic process it should be possible to determine the dose to an integrative type of imaging system and terminate the exposure when a predetermined dose is reached. If this can be accomplished economically and reliably, then the cost of radiography could be reduced along with an improved, consistent image quality.

Four major methods of exposure-time estimation are now in general use. Each of these methods require certain information to be known or be determined empirically to some degree of certainty. These methods are:

- The graphical method
- The "slide rule" method
- The calculational method
- The best guess method

Each of these methods has certain advantages and limitations in use.

The graphical method employs information generated by empirical data points for a specific source, material, geometry, and imaging system. This technique is effective when large numbers of radiographs are required of a known object under similar conditions. Figure 1-1 is a typical graph used in industry. In this case the source intensity must be known to determine exposure time. This method is limited by the operator's ability to follow lines, to interpret the graph properly, and to interpolate between given data points or lines. Also, variations in technique and film produce different results from those desired.

A second method of exposure time determination employs a "slide rule" device. This simple method requires the operator to align certain data points on the device that correspond to the particular case involved by manipulating the slide bars. This is

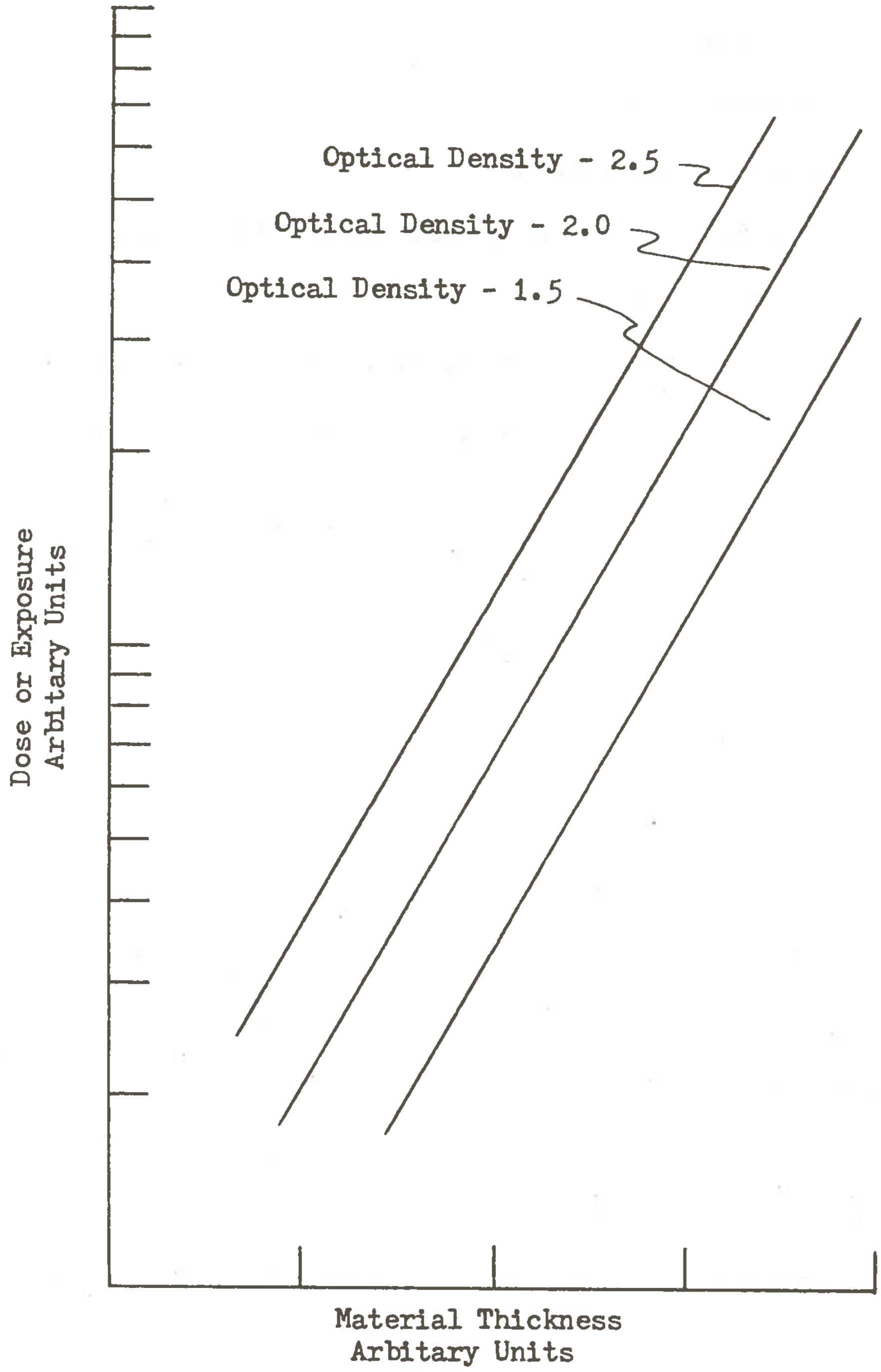


FIGURE 1-1

Typical Exposure Curves

a quick method that can be easily employed by relatively untrained operators. Once again, slide rule devices are usually for specific materials requiring operator interpolation if another material is being tested. This method assumes the original design accuracy of the slide rule is maintained under potentially adverse operator handling and neglects variations in technique and film.

The calculational approach involves solving a mathematical formula 1/. The following is a typical example:

$$t = \frac{f(D)(d_1 + d_2)^2 \exp(ux)}{S}$$

where; t - Elapsed exposure time

S - Source activity (disintegrations/second)

$f(D)$ - Film factor

d_1 - Source-to-specimen distance (centimeters)

d_2 - Specimen-to-film distance (centimeters)

-or-

Specimen thickness (centimeters)

u - Absorption coefficient (centimeters^2/gram)

x - Specimen density-thickness (gram/centimeters^2).

This approach requires a table of film factors, such as in Table 1-1 2/. The awkwardness of computational methods limits use in a number of practical applications.

The best guess approach is of questionable value but it is sometimes used in practice. The radiographer simply guesses an exposure time based upon past experience and knowledge. The direct costs of such a method include the cost of making additional

TABLE 1-1

Film Factors

Radiography source	Film type	Film Factor, $10^9 cm^{-2}$, for; Film density of 1.5	Film desity of 2.0	Film density of 2.5
^{60}Co	Eastman AA	8.6	16.0	48.0
^{60}Co	Eastman M	52.0	70.0	116.0
^{60}Co	Ansco A	8.3	14.0	45.0
^{60}Co	Ansco B	52.0	69.0	114.0
^{137}Cs	Eastman AA	7.3	13.0	41.0
^{137}Cs	Eastman M	44.0	60.0	99.0
^{137}Cs	Ansco A	24.0	39.0	128.0
^{137}Cs	Ansco B	148.0	200.0	320.0
^{192}Ir	Eastman AA	23.0	42.0	130.0
^{192}Ir	Eastman M	140.0	190.0	315.0
^{192}Ir	Ansco A	22.0	37.0	120.0
^{192}Ir	Ansco B	140.0	186.0	305.0

radiographs to insure some measure of quality. Indirectly, costs are incurred when an unknowing user of these radiographs may reduce his organization's reliance on the technique because of poor image quality resulting in higher overall costs to all concerned.

One solution to these problems of exposure-time determination is to construct a preset, alarming, dosimeter to indicate when the desired exposure is reached. Newer electronic components, particularly integrated circuits (IC), may allow such an instrument to be constructed economically. A number of new low-cost, low-power-consumption survey instruments have been introduced recently 3/4/. Also, instruments have been described that accomplish dose or exposure determination for X-ray radiography systems 5/. However, to the author's knowledge, no commercially available instruments meet the specific needs of the general radiography market.

This paper will attempt to describe an instrument to fulfill the radiographer's need for a preset, alarming dosimeter.

CHAPTER TWO

DESIGN CRITERIA

Certain general design criteria were immediately identified for a practical instrument to meet the general needs of the radiographer. Physical and electrical specifications of a general nature are as follows:

- The instrument must be composed of two sections that can be separated by at least thirty feet.
- One section of the instrument is a detector head assembly to be positioned near the imaging system detector assembly (a film pack).
- The main instrument section will have to receive signals from the detector head and shall have all relevant operating controls.
- The instrument power supply must be adequate for ten hours of continuous operation.
- Readily available batteries will be used if they have to be periodically replaced.
- The instrument must have an alarming feature that indicates when a preset dose or exposure is reached.
- Both visual and audible alarms should be provided if possible.
- The total instrument package should be of such a size that

it can be easily handled by an operator carrying other normal radiographic apparatus.

- * The cost of the instrument parts should be comparable with other survey instrument costs so that it could be an economic reality for radiography.
- * All controls and readouts should be easily understood by the operator.
- * The potential for ruggedizing the instrument should be considered in the design process.
- * The design should be based on the use of radioisotopic sources including ^{137}Cs, ^{60}Co, and ^{192}Ir.
- * Total exposures ranging from twenty milliroentgen (mR) to twenty roentgen (R) will be the design basis if these can be reasonably achieved.

From these general design guidelines the basic physical system was visualized as being a large main instrument pack connected to a smaller instrument pack via a cable of greater than thirty feet in length. All operating controls, with the exception of the detector-head power supply switch, would be included on the instrument mainframe.

To accomplish the desired dose integration, the electronic system must necessarily include the following subsystems:

- * A detector for sensing the radiation impinging on a film pack imaging system.
- * An input conditioning amplifier to condition the detector signal properly.

- * A signal integration system to integrate the conditioned detector signal.
- * A random access memory capability that can be readily accessed by the operator to enter the desired exposure dose.
- * An alarm indicating when the desired dose is reached or exceeded.
- * A system power supply providing all required voltages at the required current outputs.
- * A display indicating the total accumulated exposure.

Figure 2-1 is a block diagram of the basic system required.

Several detector types must be considered. These include solid-state detectors, ion chambers, scintillation detectors, and Geiger-Muller (GM) detectors.

Solid-state or semiconductor radiation detectors offer a number of advantages in this application. The advantages include small physical size, low-voltage bias supply, and energy-independent response. However, this is offset by the high cost of the detector system which includes an expensive input amplifier.

The advantages of an ion chamber are similar to those of a solid-state detection system except the ion chamber would be physically large and has a small output signal. This detector type would also require a sensitive, high cost input amplifier.

The scintillation-type of detector system would offer the advantage of high-speed counting in high radiation fields. The input amplifier specifications would not require a high-cost amplifier. But, this type of detector requires a highly regulated

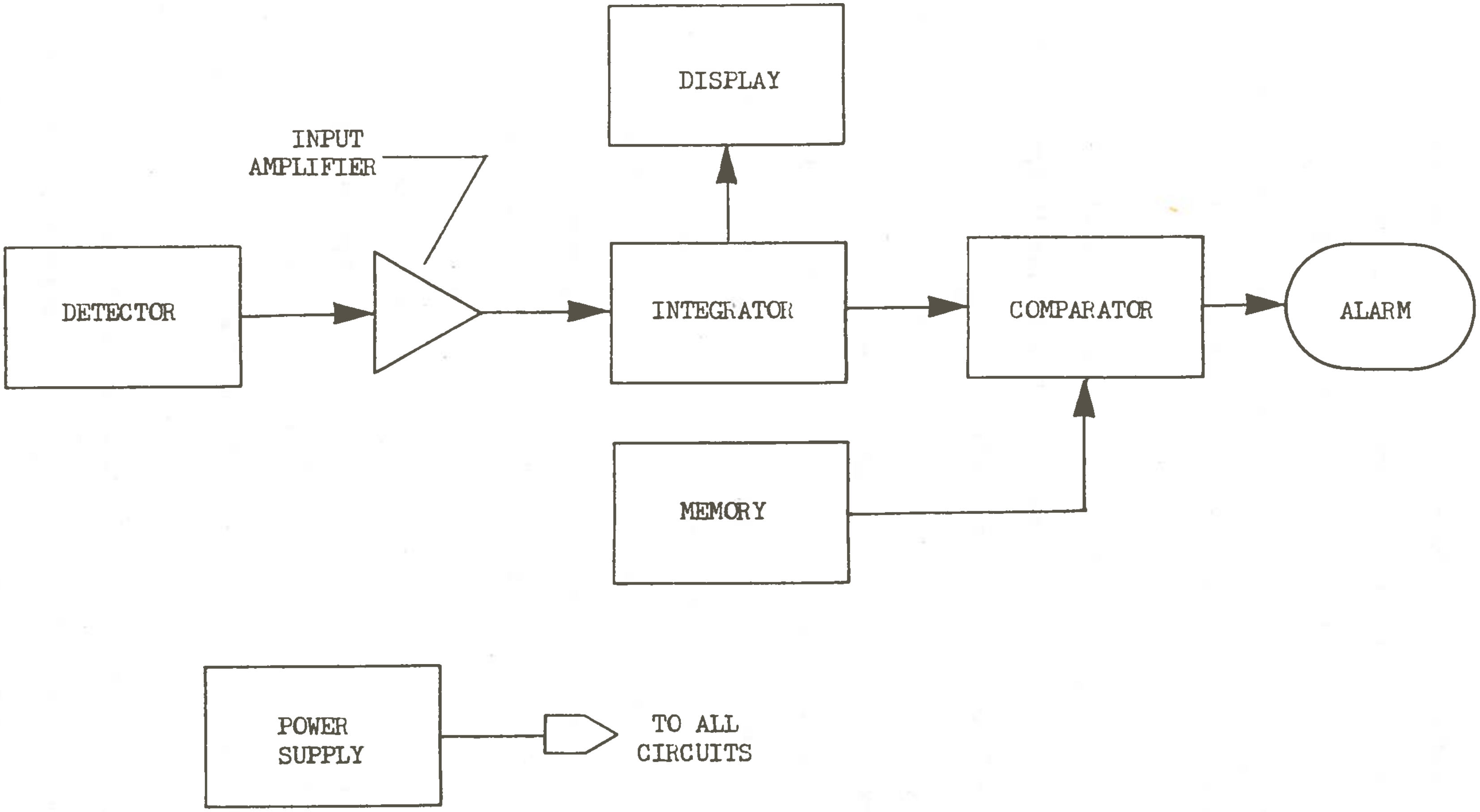


FIGURE 2-1

System Block Diagram

high-voltage power supply system producing approximately 900 volts. Also, the photomultiplier gain is extremely temperature sensitive and is affected by electrical fields.

Primarily because of the cost disadvantages of the detector systems described above the GM tube was chosen as the detector. The GM tube has a number of advantages for this application. The tubes are relatively rugged and unaffected by environmental changes such as temperature. The high-voltage supply does not require extreme stability to insure satisfactory performance. The output of the detector is a large pulse which is readily shaped for processing. Varying sizes and shapes of GM tubes are commercially available at a relatively low cost (approximately $20.00).

The disadvantage of the GM tube includes the requirement for a high-voltage power supply. Also, the tube response is energy dependent. The energy dependence requires the instrument to be calibrated for the specific energy and energy spectra of the source being used. Pulse pair resolving time is slow, limiting the counting rates that can be used. A typical energy response curve of a GM instrument is shown in Figure 2-2 6/.

The input amplifier must amplify and shape the pulse. The design of the amplifier should insure a sufficient bandwidth and sensitivity to accomodate the GM signal. This type of amplifier is well documented in the literature.

The input amplifier should then feed a pulse-shaping circuit to insure that a signal of sufficient amplitude and duration is available for processing. A monostable multivibrator is a typical

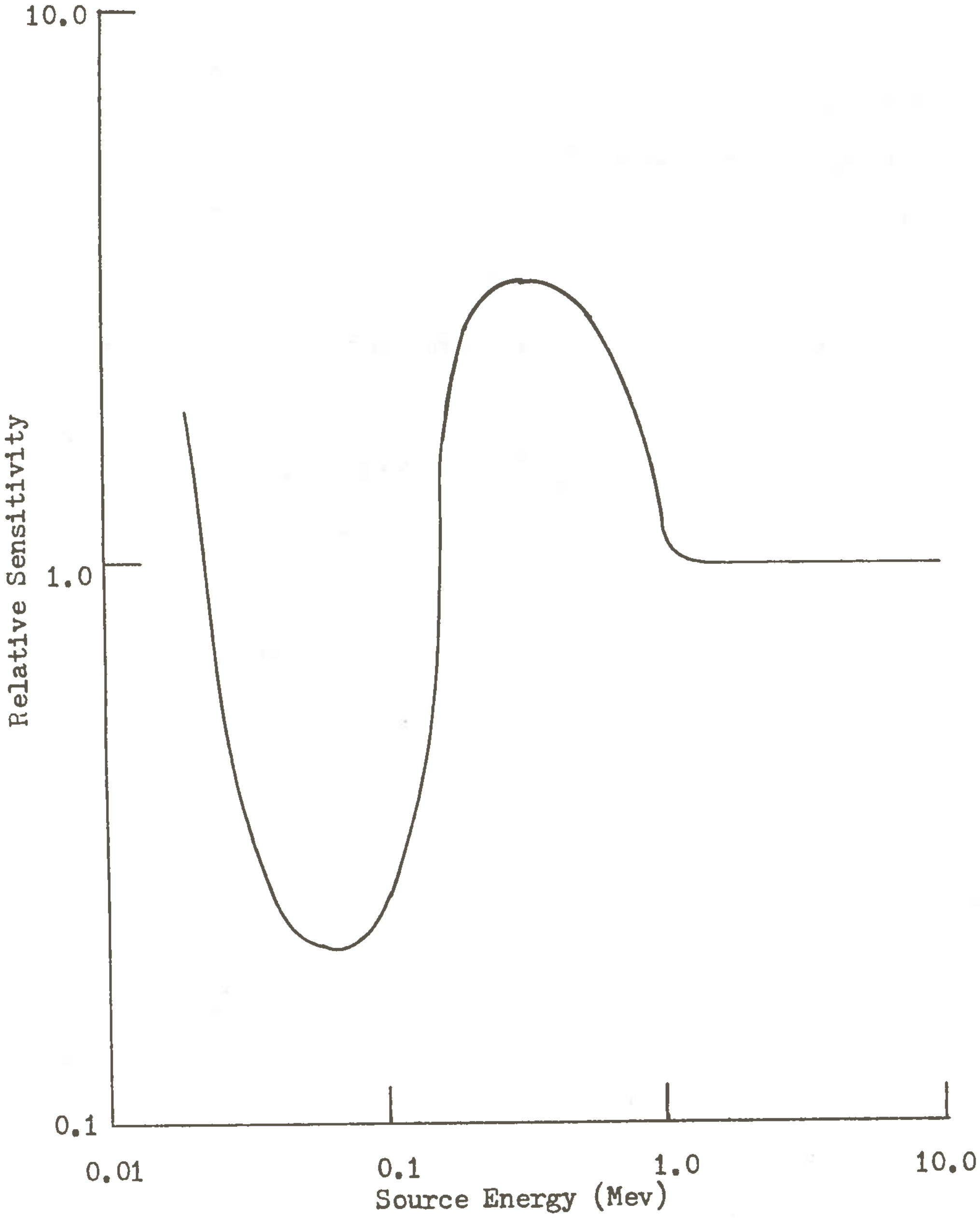


FIGURE 2-2

Typical Energy Response of GM Tubes

circuit for accomplishing this in most GM-based instruments.

The input pulse characteristics must be analyzed before the monostable multivibrator, or "one-shot", can be designed. Figure 2-3a is a typical pulse pattern from a GM tube. The pulse is fed to the input amplifier through a decoupling capacitor yielding the input pulse shape as in Figure 2-3b.

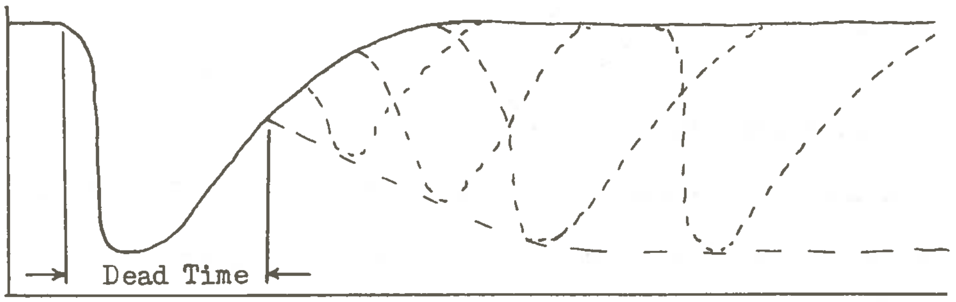
After processing by the input amplifier the pulse shape is of a square nature, as in Figure 2-3c. This pulse is fed to the input of the "one-shot". The "one-shot" insures a pulse of constant duration and amplitude as required by the signal processing circuits.

Three basic methods of using the output of the "one-shot" must be considered. They are:

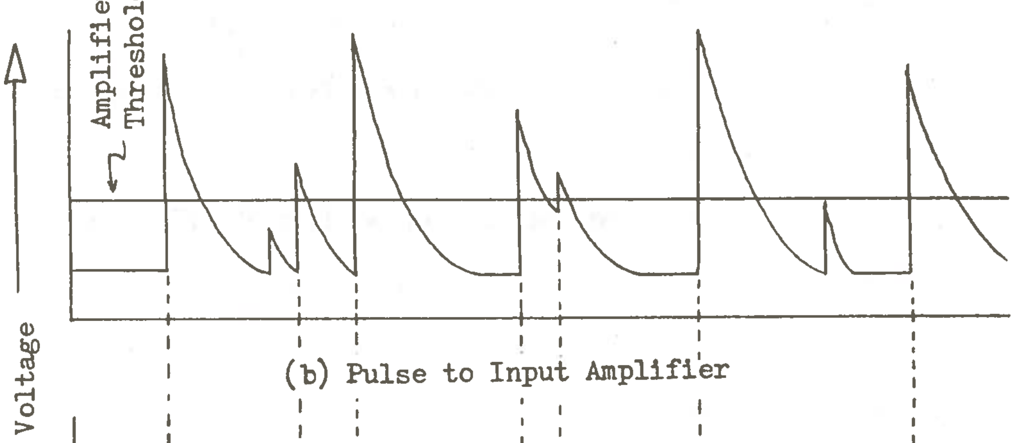
- Total analog
- Digital
- Hybrid

The total analog approach uses a circuit technique to shape and integrate the GM tube output pulse. The integrator output is compared by analog methods to a given voltage level that represents the exposure dose required. When the exposure is reached the comparator provides a signal to the alarm circuit.

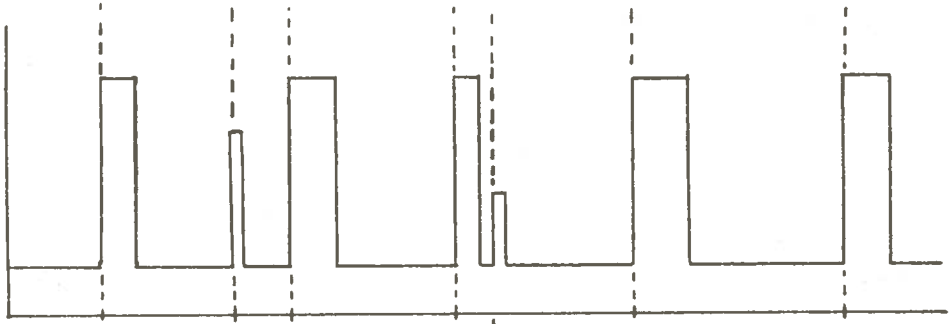
The digital approach involves counting the output of the "one-shot". A comparator output results when the dose count exceeds an appropriately scaled exposure dose count. Also, the "one-shot" output may be scaled digitally, which would provide the comparator with a count number that represents the dose in



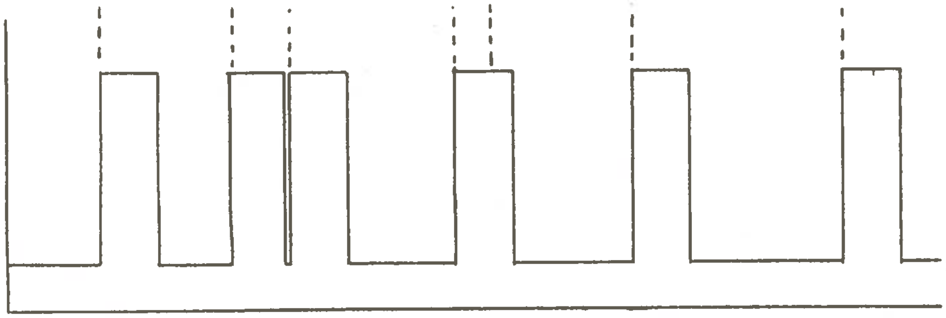
(a) Typical GM Output



(b) Pulse to Input Amplifier



(c) Pulse Output of Input Amplifier



(d) Output of Shaping Amplifier

FIGURE 2-3

Typical Pulse Shape in a GM Tube Based Counting Instrument equivalent dose units.

A third approach is the hybrid method. It differs from the digital method by using analog techniques to achieve the scaling function. A resetable integrator accomplishes the scaling by varying the reset voltage level. The scaled output is counted and compared by digital techniques.

Because of the ready availability of low-cost digital circuits, the digital method is considered the best alternative for this instrument. The hybrid method may be the best in practice, since the equipment calibration technique would be similar to those for existing equipment and would not require technician retraining.

The next major consideration is the digital-logic-family type to be used in construction. Transistor-Transistor-Logic (TTL), Resistor-Transistor-Logic (RTL), Complimentary Metal-Oxide-Semiconductor Logic (CMOS), and other logic families are readily available. TTL is probably the most available, lowest cost family offering the widest range of circuit functions available.

TTL offers the following four advantages:

1. Low cost
2. Wide variety of functions
3. Ready availability
4. High speed, typically 20 MHz

But the following disadvantages make the TTl option generally unacceptable for this project:

1. High power consumption, typically 10 milliwatts (mW)/gate
2. The requirement for a regulated power supply,

5 volts ± 0.5 volts

3. Relatively low noise immunity, typically 1.0 volt

CMOS logic is being widely introduced into the market, making it an attractive alternative (November 1973). The following advantages make CMOS particularly useful for this application.

Five advantages are:

1. Low power consumption, typically 10 nanowatts (nW)/gate
2. Large-scale integration (LSI) of circuit functions
3. Good availability from major electronic supply houses
4. Wide range of power-supply voltages, typically 3 volts to 15 volts
5. High noise immunity, typically 45% of the supply voltage

Three disadvantages are:

1. The low speed of operation, typically 5 MHz
2. Higher relative cost than TTL
3. The susceptibility of CMOS to damage by static electrical discharge, requiring special handling during assembly

For this application high-speed counting is not required. The maximum speed is determined by the detector response. Since small GM tubes have a minimum typical dead time of approximately 15 microseconds, the maximum operating frequency is found by the following formula:

$$\text{Maximum Frequency} = \frac{1}{\text{Dead Time}}$$

$$= \frac{1}{15\,(10^{-6})\text{ seconds}}$$

$$= 6.67\,(10^{4})\text{ Hz}$$

Therefore, the expected maximum frequency of operation does not exceed the typical counting speed of CMOS logic.

In November 1973 CMOS logic was approximately three to five times more costly than TTL for equal logic functions. The electronics literature at this time indicated a potential drop in CMOS price as both demand and production increased 7/. Because of LSI, CMOS offers circuit functions not available in TTL. The availability of additional functions and the potential for price decreases offset the difference in cost. In the long run, CMOS could be less costly than TTL.

All areas of electronics are concerned with the potential for damage caused by static discharges. In the Baton Rouge, Louisiana area, static discharges seldom occur because of the high humidity. Since the project will be constructed in the Baton Rouge area, no special precautions need to be taken during construction. This minimizes the impact of the static discharge disadvantage.

CMOS disadvantages pose only minor or irrelevant problems in the design and construction of the proposed instrument. The advantages and minor impact of the disadvantages of CMOS make CMOS the logic family best for this instrument.

The display of the memory and counter counts, which are in digital form, can be accomplished through the use of one of the many types of digital displays. Alternatively, a digital-to-analog conversion may be performed on the data and the resultant displayed using a conventional analog meter.

Among the digital displays available are the gas discharge, incandescent, light emitting diode (LED), fluorescent, and liquid crystal types. Gas discharge and fluorescent displays were dropped from consideration since they require a high-voltage supply.

Among the remaining display types, LEDs were chosen for their low price and good availability. Liquid crystals have the lowest power dissipation of any display types, but are costly in small quantities. Incandescent displays are moderately priced but have short lives and higher power consumption than LEDs. See Table 2-1 for a comparison of display types 8/.

The power supply must have both high-voltage and low-voltage sections; the high-voltage section must supply 500 to 600 volts at 20 milliamperes (ma). The low-voltage section must supply the proper voltage for the digital and analog circuit operation. The primary power source must be readily available batteries.

In retrospect, price and availability of components dictates their use in this project. Because of this, thecircuit designs chosen are relatively economical, but not necessarily the most economical or the technically best choice for performing a given job. However, the design criteria may be met at a relatively low cost.

TABLE 2-1

A Comparison of Selected Seven-segment Display Parameters

	Light Emitting Diodes	Liquid Crystals	Gas Discharge	Vacuum Fluorescent	Incandescent
Sustaining Costs	Low	Low to Moderate	Low to Moderate	Low to Moderate	Low to Moderate
Operating Speed	Nanoseconds	100 ms on, 300 ms off	Microseconds	Microseconds	Milliseconds
Power Dissipation/Digit	200 mW	40 μW	400 mW	250 mW	1.0 W
Reliability	Excellent	Good	Good	Good	Good, Ind. Fil. Failure poss.
Safety	No Problem 5 Volts	No Problem 30 Volts	Requires Care 200 Volts	No Problem 30 Volts	No Problem 5 Volts
Brightness	20-100 ft. Lamberts	Light source Required	50-400 ft. Lamberts	80 ft. Lamberts	1000-10000 ft. Lamberts
Environmental	Rugged	Breakable Glass	Breakable Glass	Breakable Glass	Breakable Glass
Cost/Digit - Driver, Power Supply Incl.	$7-15	$5-12	$11-16	$3-9	$6-40

CHAPTER THREE

INSTRUMENT DESIGN AND CONSTRUCTION

The design and construction of the instrument was begun using the guidelines presented in Chapters One and Two. Because of the low power consumption and LSI, CMOS was chosen for the construction of this instrument.

Design

A literature search of manufacturer's catalogs was carried out to determine price, availability, and delivery times for CMOS ICs. The majority of CMOS ICs available in late 1973 were manufactured and distributed by RCA through major electronic supply houses. Prices for small quantities of CMOS ICs were two-to-five times greater than the 100-lot quantities. A number of surplus or hobby electronic firms had limited quantities of certain circuits available at lower than manufacturer's unit quantity prices. Suppliers of components for the project were determined by price and availability.

Simultaneously, circuit designs were considered. The major problem areas were the design of an appropriate memory circuit and an integrating circuit. Because of the extensive literature available on high-voltage power supplies and input circuits, they were not considered to be a major problem area.

Potential counting (or integrating) circuit design problems were solved by using a Solitron CM4102 (See Appendix C). The

IC contains a $3\frac{1}{2}$ digit counter, latches, multiplexed binary-coded-decimal outputs, and reset capability in a single Dual-in-line package (DIP). The maximum count rate is approximately 800 KHz. The CM4102 may be operated on a single supply voltage between 3 and 7 volts. The maximum CM4102 supply voltage is generally lower than most CMOS circuits, which requires care to be exercised so as not to exceed the maximum voltage limit.

The memory circuit requires that the operator have access to the memory to enter new exposure doses and to observe the dose information set into the memory. Two basic memory types were considered, electromechanical and solid-state.

The electromechanical memory configuration could consist of either rotary switches, thumbwheel switches, or matrix switches. This type of memory requires a greater volume within the instrument, and therefore increases the physical package size required. Switches would require hermetic seals to be useful in a practical system which would greatly increase the cost of the switches.

Solid-state memory systems do not directly provide an indication of stored information unless peripheral equipment is added. In this case a display is required for an accumulated count indication. It is possible to display memory or accumulated count information by gating the desired count with AND-OR select gates. The solid-state memory was chosen because of small size, low cost, availability of a display system, and system compatibility.

The count entered is determined by a decade counter that may be advanced by the operator depressing a push-button switch. The push-button switch allows the clock signals to advance the counter. Once all desired digits are entered into the memory, the function switch is returned to its normal operating position, which does not allow any other information to be entered into the memory.

The BCD-to-seven-segment decoder has a blanking capability to reduce power consumption. During initial testing the display is not blanked. The final instrument display is blanked until the "display" push-button is depressed.

Basic Instrument Construction

The dosimeter sections described above were assembled on a pre-drilled phenolic circuit board. The ICs were mounted by soldering solid wire interconnections to the package leads. Because of the difficulty in changing the circuits, the circuits were removed and reinstalled using IC sockets. This facilitated removal, modification, and replacement of ICs and discrete components.

The circuit described functioned as expected. Certain logic signals required inversion for proper operation because of incomplete CM4102 specifications. Figure 3-1 is a block diagram of the circuit as tested.

Instrument Modifications

Several instrument modifications were incorporated into the basic system to extend the system capabilities. The following section describes these modifications.

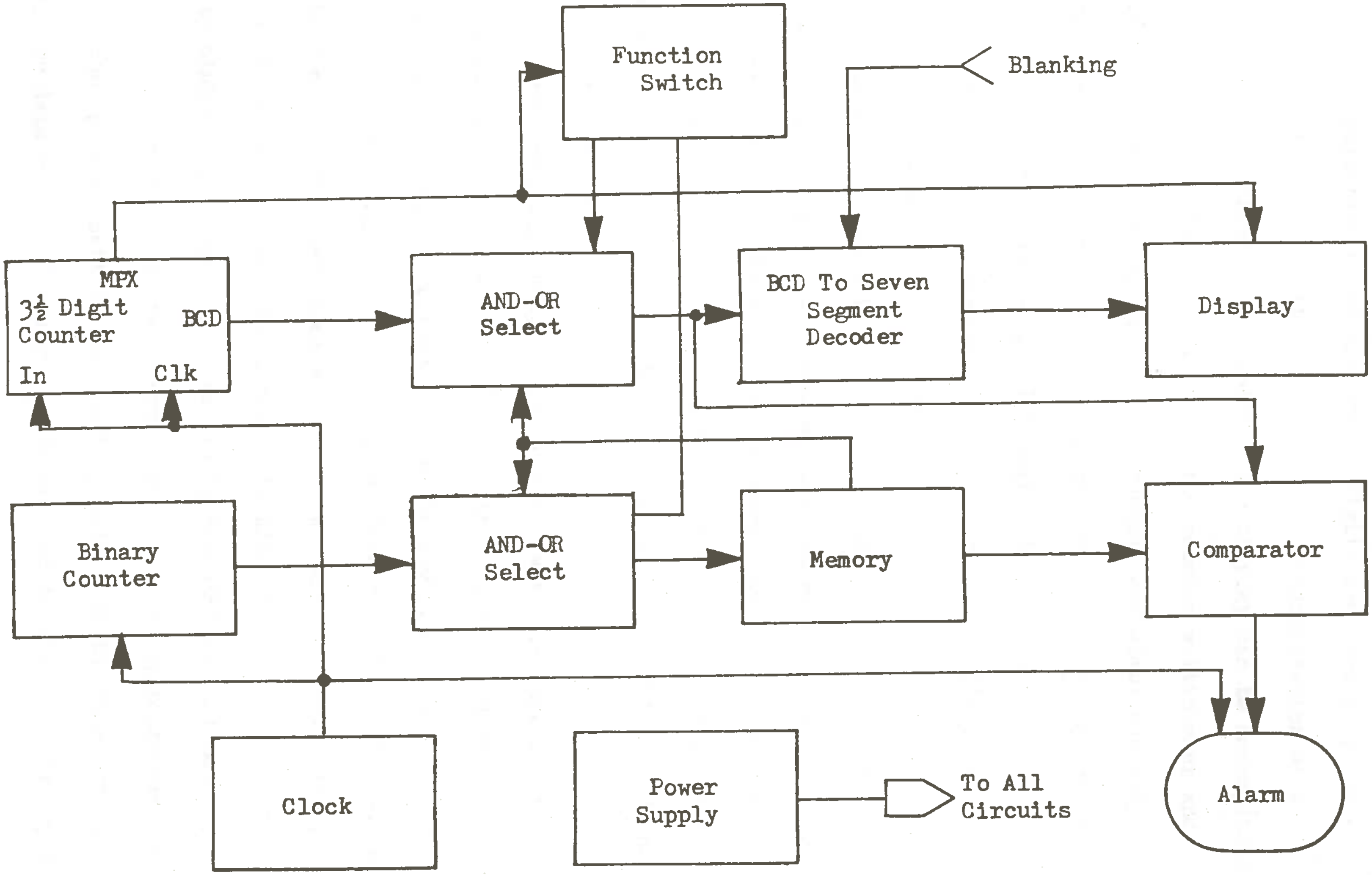


FIGURE 3-1 Block Diagram of Primary Electronic System

The multiplexing of the CM4102 digits requires a system clock to drive the multiplex circuits. Synchronization of memory address and counter digits feeding the display can be accomplished by using the system clock to drive the counter multiplexer and memory-address code generator continuously and simultaneously. By synchronizing the memory and counter BCD data, the output of each may be compared using a BCD magnitude comparator.

The digits are scanned from most significant digit to least significant digit in order. At the start of the comparison cycle the comparator output is reset. The comparator-output state is changed only when the accumulated count exceeds the preset count by one count. If the output state changes when the counts are equal, the alarm would be activated if the count is zero and the memory is reset. This condition would cause operator confusion and inconvenience.

The comparator feeds a NAND circuit which is also fed by the system clock, the instrument function switch, and other logic signals. The clock operates within the low frequency range of human hearing and provides the alarm drive frequency. The alarm is composed of a permanent magnet speaker and LED combination, providing both visual and audible signals. The alarm is driven by high current logic circuits fed by the NAND circuit output.

The preset exposure information is entered into the memory by the operator setting the function switch to the position to allow data entry. The digit to be entered is also selected by the function switch. The switch controls data entry into the memory.

The next step in testing was the addition of the survey meter function to the instrument. This function is not required by the design criteria. However, a radiographer is required by law to have a survey meter available. A minor extension of the basic system design will provide the survey meter function.

Figure 3-2 is a block diagram of the additional circuits. Only the addition of two gate packages, a seven-stage binary counter, and a delay circuit (a dual "D" type flip-flop) are required.

Figure 3-3 is a timing diagram of the survey meter logic. The survey meter function is easily implimented. The output of the GM tube is a random series of pulses (see Figure 3-3a). Dose rate is proportional to the average number of pulses per unit time. Therefore, if the counter is enabled for a fixed period of time, the count per unit time is displayed. Repeating this process, after resetting the counter, yields counts that are proportional to the dose rate.

To accomplish this using the CM4102 counter, it must be enabled, count latched (stored), and reset. The process must be repeated to provide a count proportional to the dose rate. Figure 3-3b,c,d is the timing of such a process. The count storage occurs at a fixed time after reset. Resetting was accomplished by delaying the latch pulse for one clock period.

The display may be scaled to read directly in units of dose by varying the count enable time. Calibration was accomplished by interconnection of various binary counter outputs to the NAND

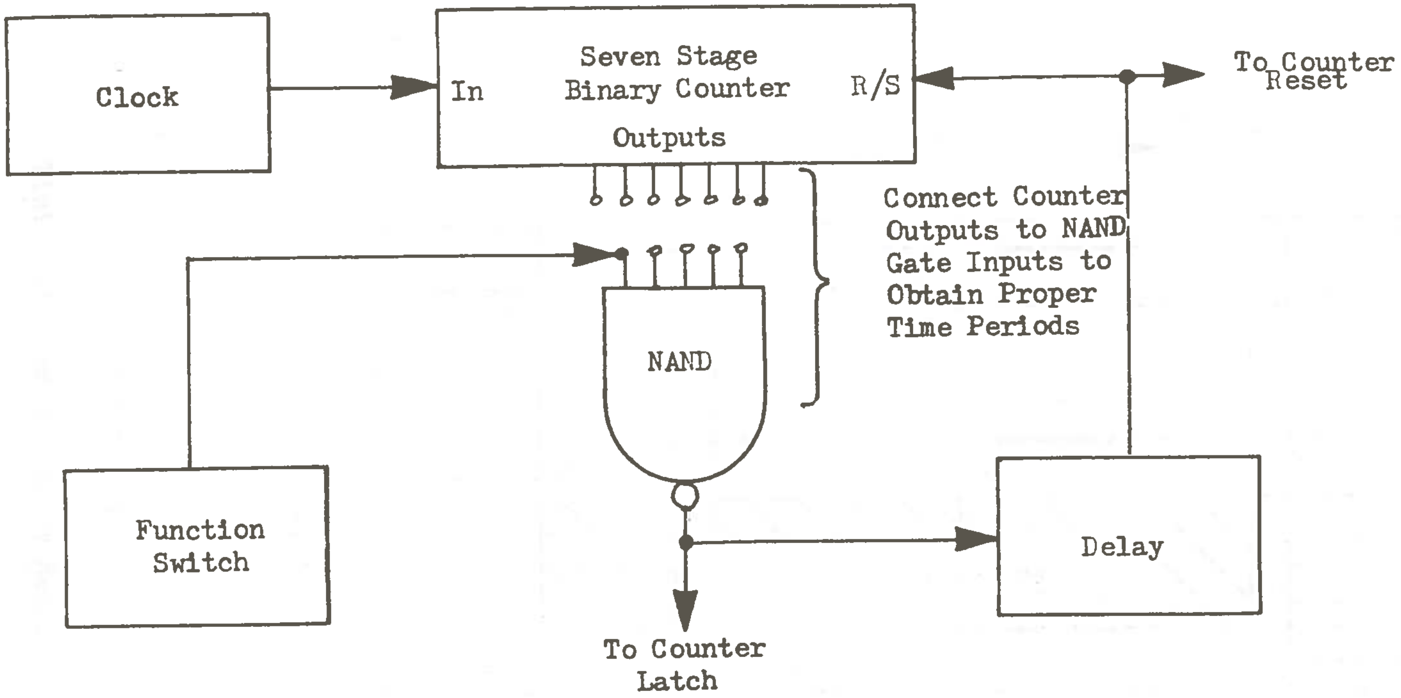


FIGURE 3-2

Components to Add Survey Meter Function to the Original Instrument

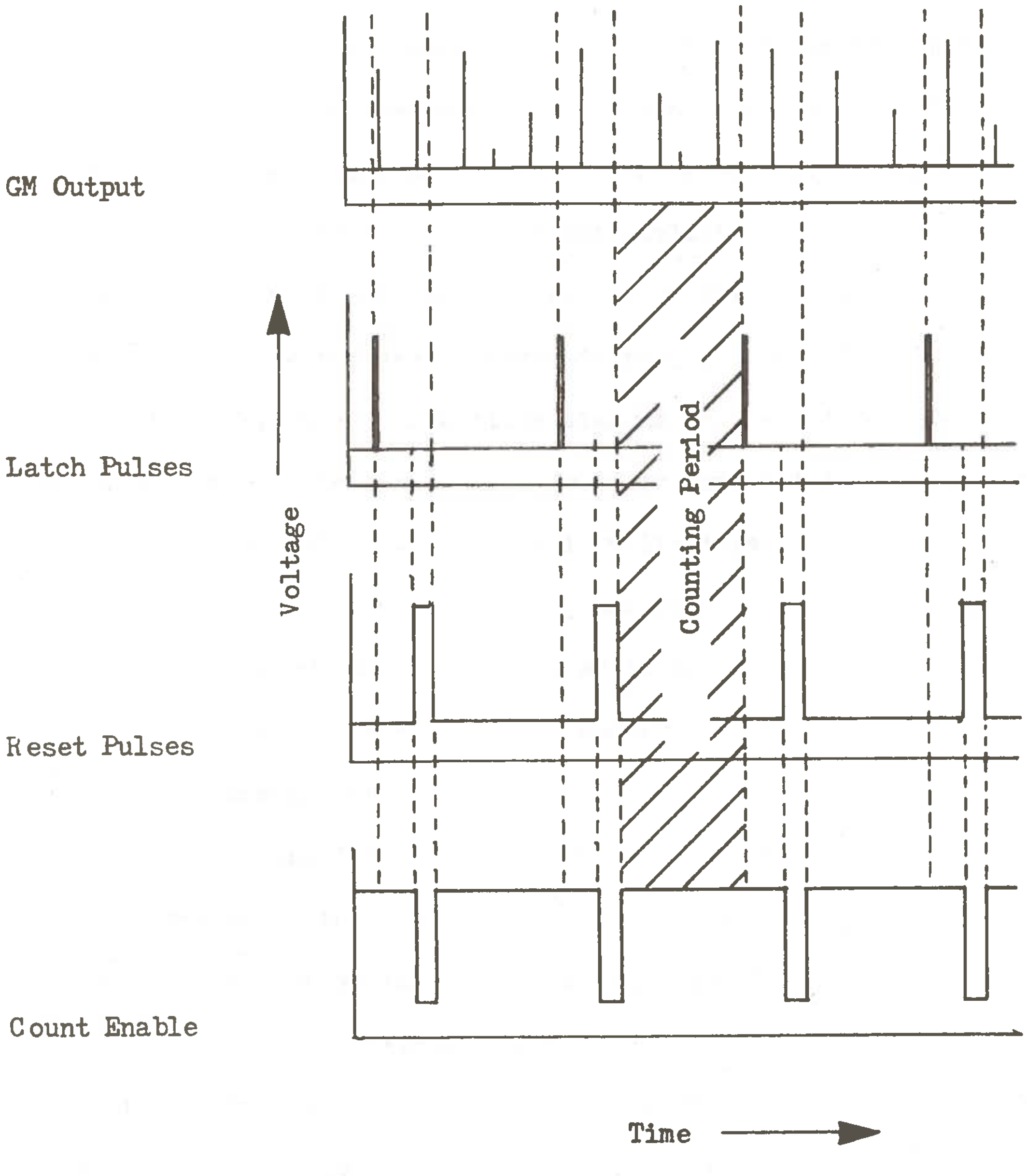


FIGURE 3-3

Timing Diagram of Survey Meter

gate feeding the latch and delay circuits.

The addition of the survey-meter function allows the instrument to be used as an area monitor. No additional major circuits (except gates) are required to perform the area-monitor function.

Prior to the addition of an input amplifier and detector system it is desirable to add the provision for scaling the input counts so that the integrated count displayed reads directly in dose units. Figure 3-4 is a block diagram of the method used. The "one-shot" shapes the input pulse prior to prescaling. The IC, MC14528, used contains two monostable multivibrators. The "one-shot" not required for pulse shaping was made into a digital-to-analog converter by adding a RC filter to the output. The converter output can drive a 0-100 microampere meter movement via a front panel banana jack.

The input amplifier construction uses CMOS transistor pairs. They are biased in the linear amplifier configuration9/.

The first high-voltage supply circuit consisted of an oscillator driving a step-up transformer. The transformer output is rectified to provide 400 to 600 volts. The first high-voltage supply did not provide the regulation required. The design was changed to include a switching regulator driving the transformer to provide the regulation required.

The GM tube was obtained from a surplus survey meter. The tube has no type number on its case, but it appears to be similar to an EON Type 5309. The operational history of the tube is unknown.

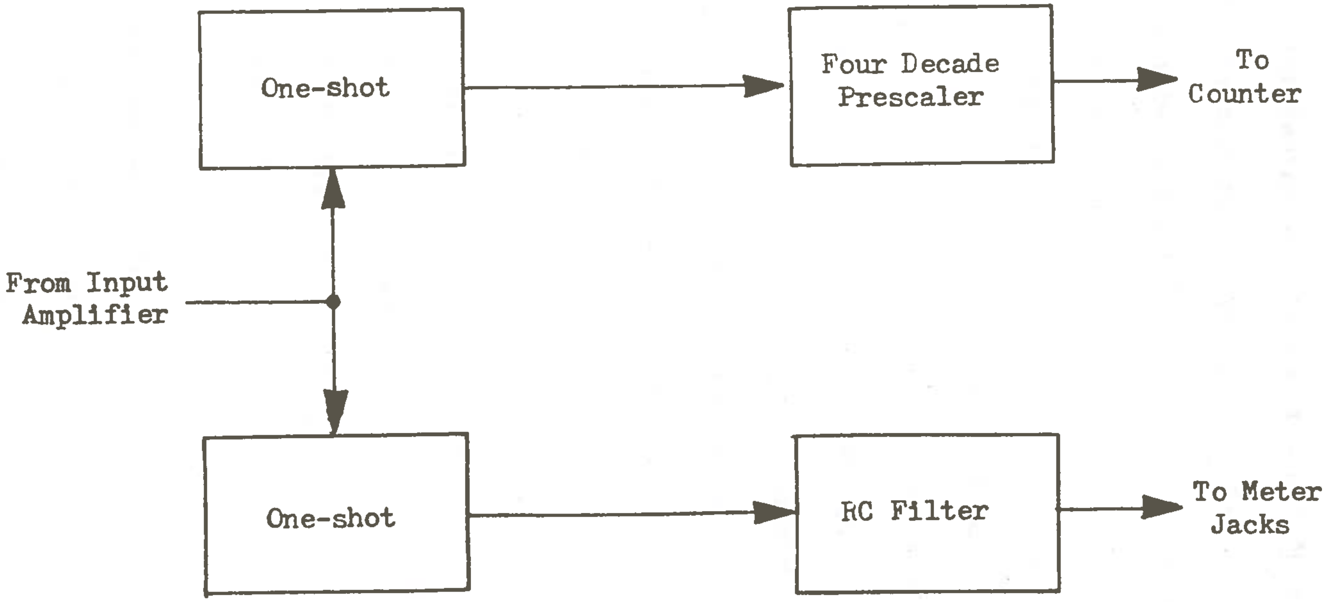


FIGURE 3-4

Block Diagram of Prescaling and Analog Meter Driver Circuits

The first high-voltage supply did not provide the regulation required. The design was changed to include a switching regulator driving the transformer to provide the regulation required.

The GM tube is required to be located at the film pack which is at least thirty (30) feet from the main instrument. Therefore, the high-voltage supply, an amplifier, and a line driver need to be constructed on a separate circuit board with a separate low-voltage power supply. See Figure 3-5 for a block diagram. The circuits used are as described previously.

The function of the driver is to provide isolation and drive capability. Since the maximum frequency of operation is expected to be less then $6.67\ (10^4)$ Hz, a shielded audio cable rather than a high-cost coaxial cable was used to connect the main assembly to the detector head assembly. The nominal output impedance is 50 ohms. A single nine (9) volt battery, controlled by a toggle switch, provides power. Quiescent battery drain is typically 2.0 ma. Two "N" type batteries, which can be replaced by a low-current zener diode, provide a voltage reference.

A scaler capability was also added because of the availability of a binary counter during construction. The counter outputs control a gate to allow count integration signals to control the starting and stopping of a displayed count. The counter is driven by the system clock. Manual control is also provided.

The instrument is mounted in a 3 in. X 5 in. X 7 in. aluminum minibox. The detector head assembly is enclosed in a $1\frac{1}{2}$ in. X 2 in. X $3\frac{1}{2}$ in. aluminum minibox. The GM tube is mounted

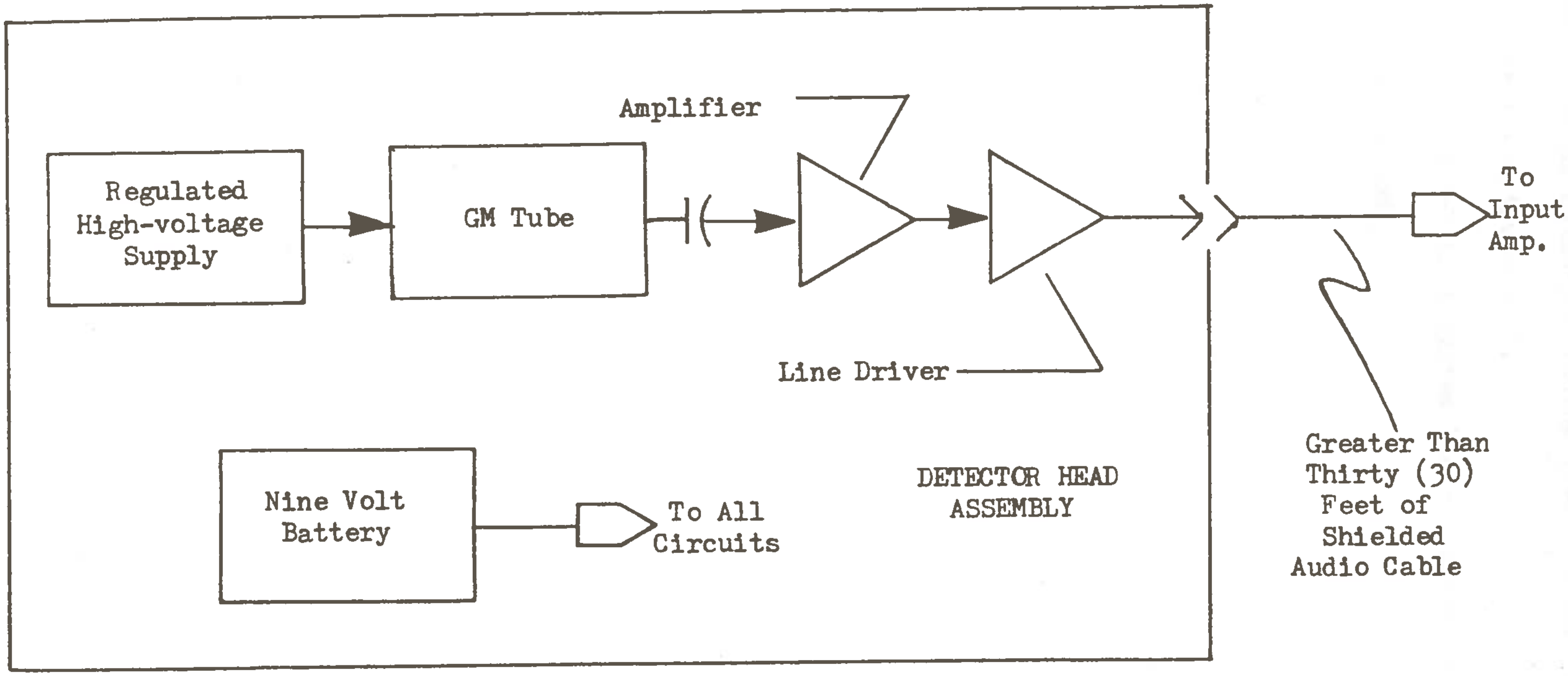


FIGURE 3-5

Block Diagram of Detector Head Assembly

on a coaxial cable protruding from the box approximately nine (9) inches (see Figure 3-6).

Figure 3-7 is a system block diagram of the complete instrument as tested.

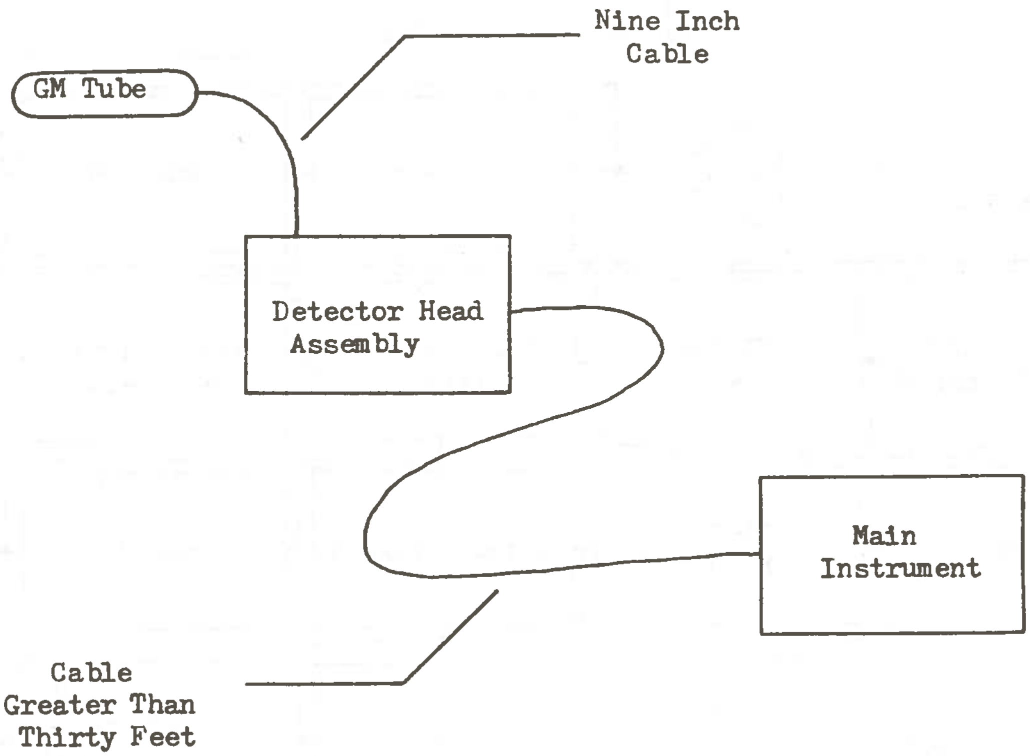


FIGURE 3-6

Sketch Relating Components of the System

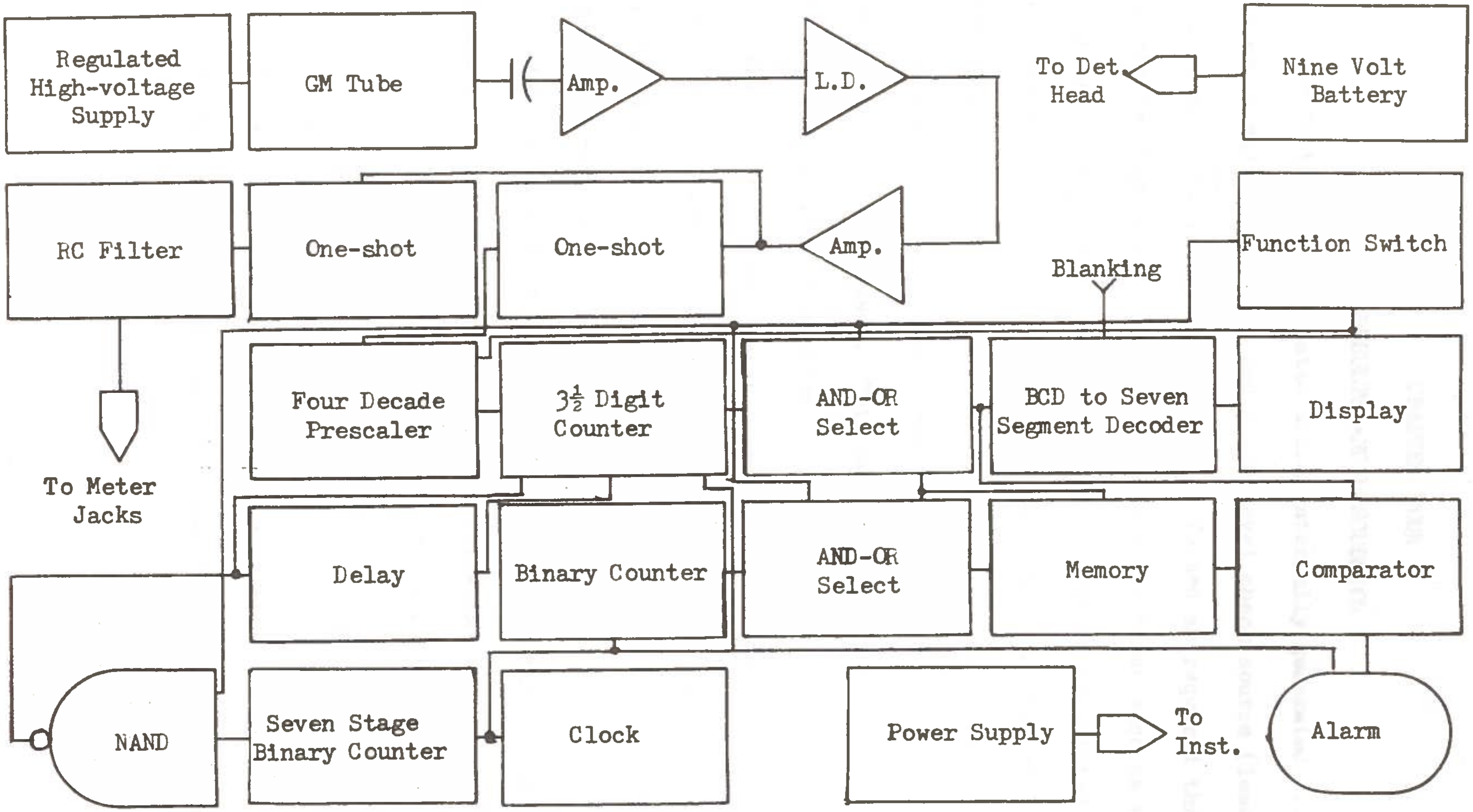


FIGURE 3-7

Block Diagram of Complete Preset, Alarming Dosimeter with Modifications

CHAPTER FOUR

RESULTS AND DISCUSSION

The instrument was tested using internally generated clock pulses, a pulse generator, and a low level check source (less than 10 µCi ^{137}Cs). The instrument performed as required throughout the testing period. Minor operational problems such as wires breaking, loose connections, and general problems associated with breadboarding a prototype instrument were easily corrected. Calibration of the survey meter function with a known source was possible.

At low radiation levels (less than 50 mR/hr) the inverse square law is rigorously followed. This made possible the calibration of the meter with known sources.

When the instrument was exposed to higher fields (greater than 1 R/hr), however, the dose rate failed to follow the inverse square law, and the display failed to return to zero when the source was removed.

The instrument's failure to perform in high fields was probably because of one or all of the following:

- The uncertain history and specifications of the GM tube
- Faulty system logic
- Dead time loses at high dose rates

The following actions could be taken to eliminate the problem:

- Obtain a tube with known specifications
- Review the logic of the entire system
- Reduce the dead time losses by:
  1. Shielding the GM tube to reduce the dose rate
  2. Obtaining a GM tube that functions at the radiation levels required

No corrective action was deemed necessary for the project because the instrument demonstrated the basic concepts set forth in Chapter One.

Since dead time corrections are encountered frequently when working in high radiation fields, a review of the dead-time phenomenon may be useful at this point. Dead time must be considered when using GM tubes because of the randomness of radioactive decay and the finite resolving time of the system. The latter phenomenon is a function of the GM tube and the counting system. The dissipation time of the space charge around the GM tube cathode limits the ability of the tube to respond during a finite time. The counting system shapes the GM tube output pulse for use by the counting circuits. The shaping circuits provide a pulse whose duration and voltage is fixed. The counter will not respond to pulses occuring during the tube dead time or the shaped pulse duration, whichever is greater. As the field intensity increases, the probability that a pulse will occur during either of these events increases. Therefore, the system count rate is not a linear function of dose rate.

Quantitatively this can be expressed by the following formula: 10/

$$\dot{n} = \frac{\dot{m}}{1 - \dot{m}t}$$

Where; $\dot{n}$ - True count rate
$\dot{m}$ - Observed count rate
t - System resolving time
- or -
GM-tube dead time

The effect of resolving time on count rate accuracy can be shown by Figure 4-1 11/. Refer to discussion in Chapter Two.

A GM tube with known specifications would allow determination of the maximum field in which the instrument may operate with a known degree of accuracy.

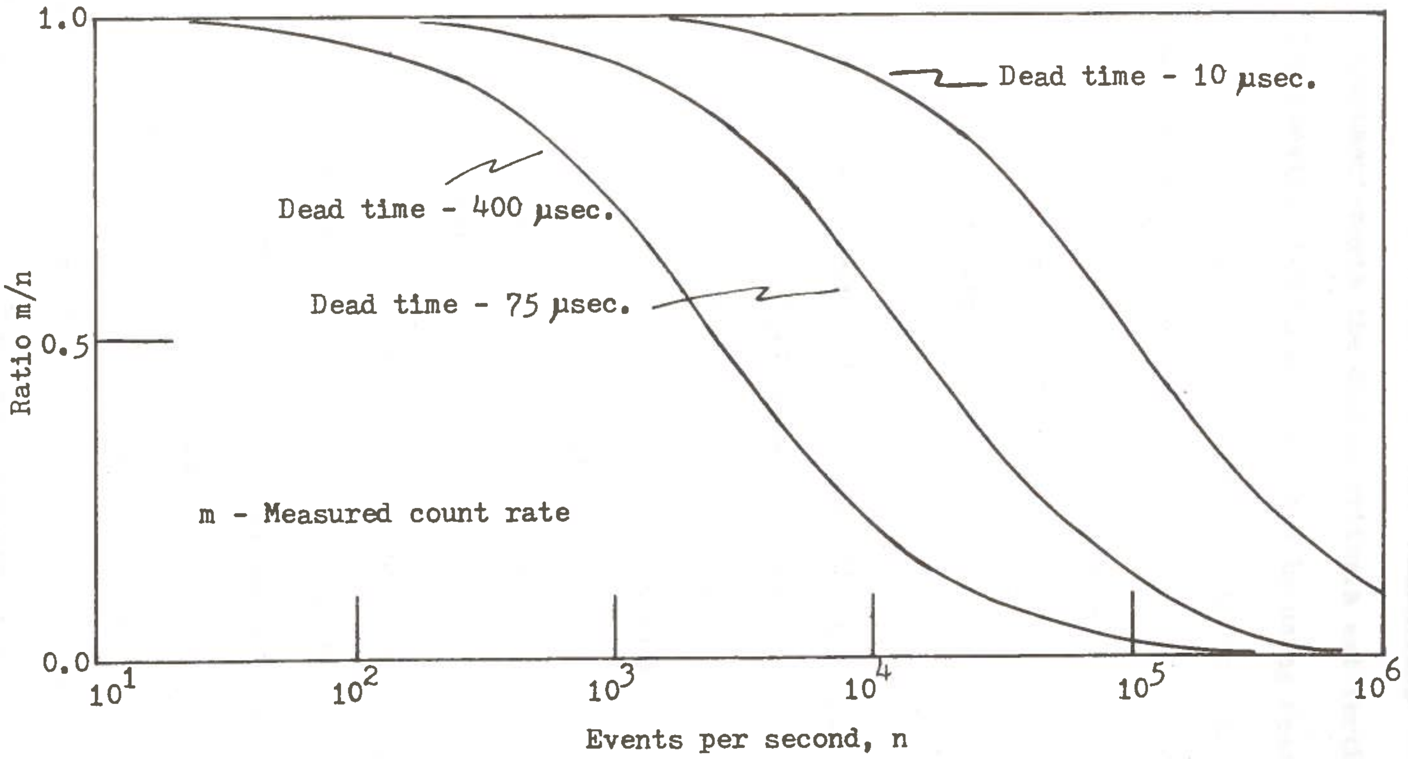


FIGURE 4-1

Dead Time Correction Factors

CHAPTER FIVE

CONCLUSIONS AND RECOMMENDATIONS

The instrument meets the design criteria set forth for the thesis. The construction is accomplished by using readily available, economically priced components. No special techniques, tools, or test equipment is required to fabricate and test the instrument. The power comsumption is low, less than 3 ma with display blanked, permitting normal continuous use for several hundred hours with 4 "AA" batteries.

The expansion of the basic instrument concept, as described in Chapter Two, demonstrates that a versatile instrument may be easily constructed from a basic counting system. The area monitor function is particularly useful. An unambiguous display with an alarm set point gives the system a major advantage over analog instruments. It should be noted that the cost of the analog type meter-relay is approximately equal to the cost of the entire digital instrument ($100).

The next phase of development should be directed toward the construction of a prototype, field-testable instrument. First, a review of the basic system logic must be accomplished, since new ICs may become available since the initial design. Second, the instrument should be fabricated in such a fashion as to facilitate field testing. Last, the prototype instrument should be field tested by both electronics personnel and radiographers to evaluate its performance.

The next instrument should include a low-cost, low-accuracy logarithmic analog meter; an audible dose rate indicator (chirper); a readily rechargeable battery supply; and a GM tube specifically suited for the radiography timing. A second GM tube with more sensitivity should be located in the main package for local surveys.

An analysis of system block diagram indicates that it is possible to construct the instrument in a modular form. The following subassemblies could be used in various combinations to form the instruments desired:

1. Mainframe composed of a
    a. Low-voltage power supply
    b. High-voltage transformer
    c. Display
    d. Counter circuit
    e. Connectors with common busing
    f. GM tube
2. High voltage regulator
3. Memory, electromechanical or solid-state
4. Alarm comparator

The modular approach would allow easy maintenance, a configuration to meet the user's needs, reduced cost to user, reduced downtime, easy upgrading as new circuits become available, and easy addition of new subsystems to expand the instrument capability.

Figure 5-1 is a simplified representation of a physical layout of the electronics package. Instrument controls could be located in each module and the instrument case would have knock-out plugs to accommodate various control configurations.

For example, a variable high voltage control section would allow the instrument to be used as a scaler with any detector.

Simply including a discriminator section would provide an expanded capability as a single channel analyser (SCA). Figure 5-2 is a block diagram of such a system.

Since the system uses digital logic, the area monitor function could be expanded to provide multipoint coverage. A digital system does not require the use of long time-constant filter circuits to obtain an average level. However, the randomness of decay may cause temporary excursions above alarm levels if the alarm level is set near the average level. The formula below can be used to evaluate the probability of the occurance of "n" given a normal distribution.

$$W(n) = \frac{m^n e^{-m}}{n!}$$

Where; $W(n)$ - Probability of event "n" occuring

m - True mean

n - Observed count

Figure 5-3 is a block diagram of such a system.

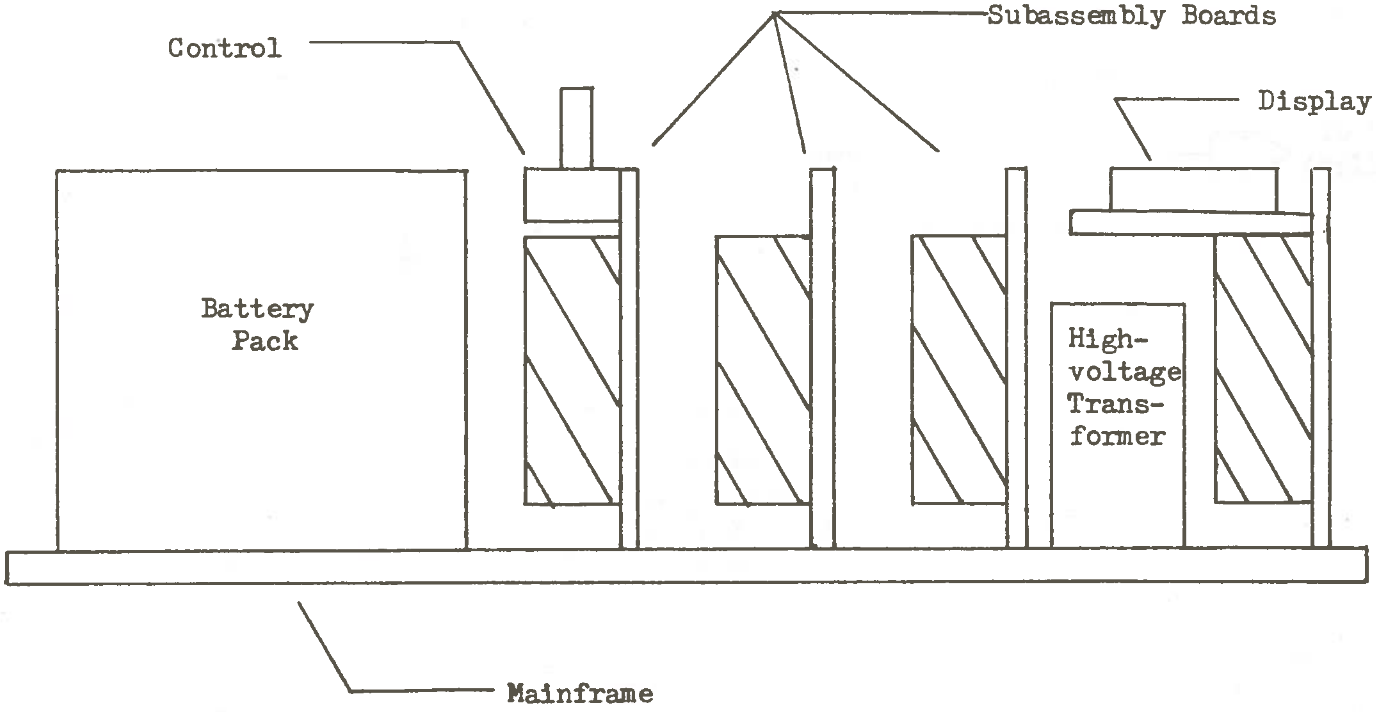


FIGURE 5-1

Side View of Instrument Using Modular Construction

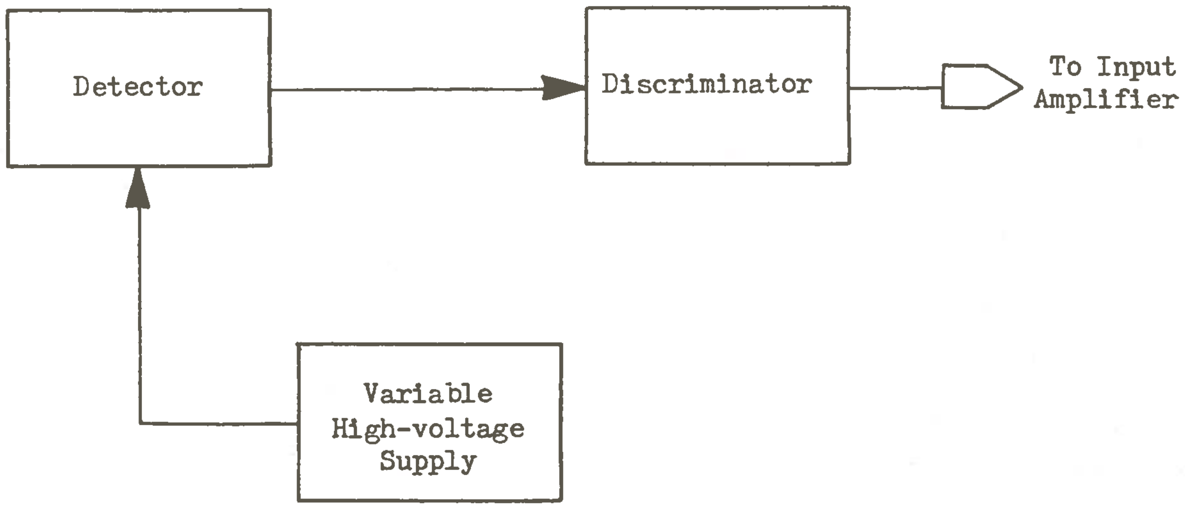


FIGURE 5-2

Single Channel Analyser Addition to Basic Instrument

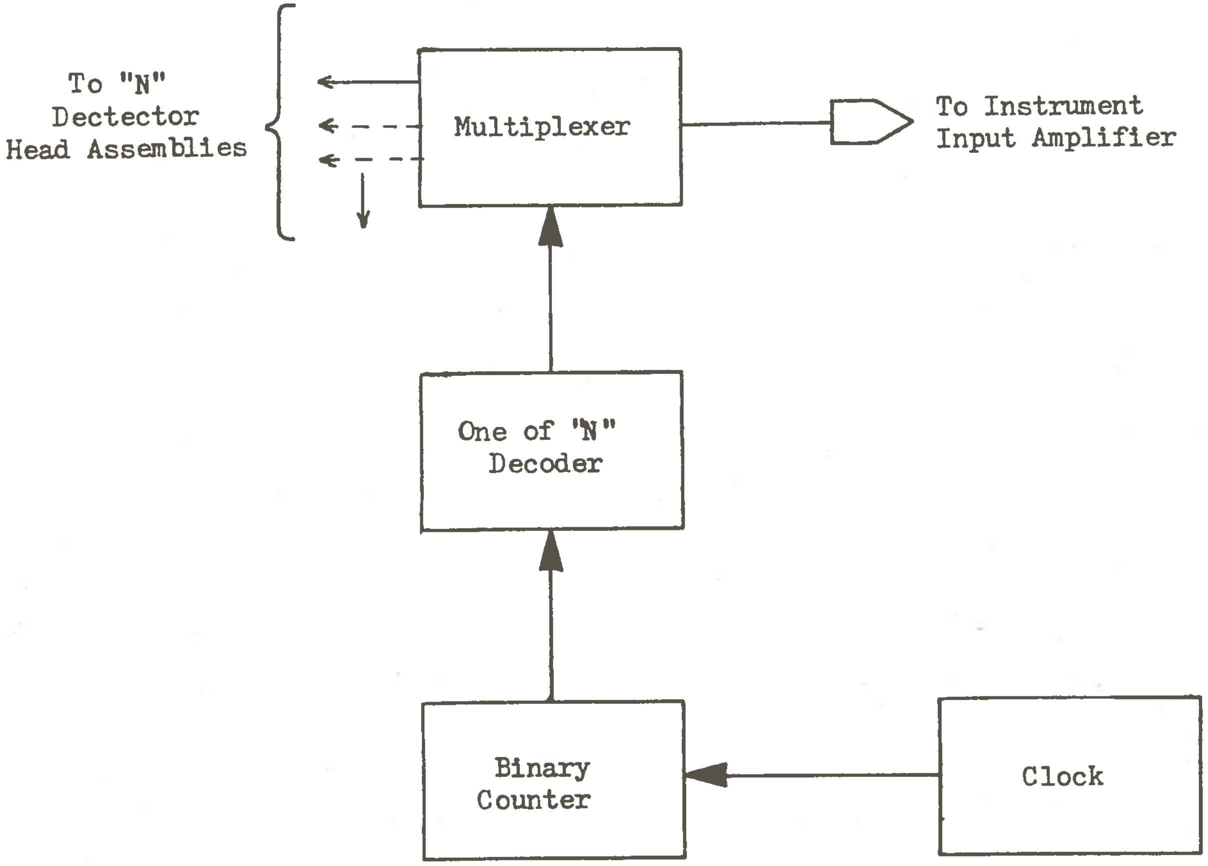


FIGURE 5-3

Multipoint Area Monitor Addition To Basic Instrument

Table 5-1 is a summary of some of the basic possibilities available using the module concept of instrument construction

TABLE 5-1

Module Requirements for Each Instrument *

INSTRUMENT

MODULES	SCA	Survey	Area Monitor	Preset Alarming Dosimeter	Multi-point A. Mon.	Scaler	Dosi-meter
Variable HV Supply	X					X	
High-volt. Sup. Fixed		X	X	X	X		X
Display	X	X	X	X	X	X	X
Mainframe with Battery	X	X	X	X	X	X	X
Discriminator	X						
Memory			X	X	X		
Alarm		O	X	X	X		O
Input Multiplexer				X			
3½ Digit Counter	X	X	X	X	X	X	X
Comparator			X	X	X		O

* - X Denotes required, O Denotes optional.

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APPENDIX A

COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (CMOS)

TECHNICAL BULLETIN NO. 1

by Irwin Lucks

This article, with some minor modifications, was written by this author in 1969. The information contained herein is still pertinent today, and is used presently at Solitron Devices, Inc., to fabricate Integrated Circuits.

Complementary MOS circuits are normally made on an N-type substrate, which necessitates the use of a P-type well for N-channel devices (Figure 1). This well must be connected to the lowest potential of the devices in the well. If additional N-channel devices are to be operated at higher potential, separate wells are required.

All FETS are enhancement mode; transconductance (g_m) is directly proportional to mobility and channel width and inversely proportional to channel separation. Because N-channel units have a higher mobility, they have approximately twice the transconductance of an identical P-channel device. Therefore, when matching the g_m, the P-channel units will have approximately two times the channel width of the N-channel devices. A protective diode is used at all high-impedance gate inputs leading to external terminals. These diodes serve to protect the device in the event of a static charge on package terminals.

In most computer circuitry, operating speed is more important than power consumption. However, in aerospace and portable (battery operated) digital system applications operating speed is less significant than power dissipation. In applications of under 10-MHz clock rates, where low power is of major importance, CMOS seems ideally suited.

Additionally, in low-power systems, only a fraction of the FETS are switching at any given time. The average digital switching element in a low-power system has an estimated duty factor of 10^{-2}. Operation of digital systems at very low powers requires a basic circuit element (or cell) which dissipates very little power in the quiescent state, i.e., when it's in the "0" or "1" condition. A capacitor is a good example of an element that dissipates very little power when either fully charged or fully discharged. It is only during the switching transient that any power is dissipated.

The total power dissipation of a switching element is the sum of both quiescent power and transient power dissipation.

The former is independent of operating speed; the latter, however, is a function of the clock rate and the voltage difference between its "on" and its "off" state. One other factor influencing power dissipation is the capacitance of the logic element. Usually this can be made sufficiently small to be only a small influence.

In conventional P-channel or N-channel MOS circuits most of the power dissipated is quiescent power because a resistance is used as a load for the transistor (Figure 2). This is true for bipolar circuitry as well. The use of a complementary pair, in which the load resistor is replaced by a FET of opposite polarity (Figure 3) results in appreciably lower quiescent power dissipation.

Because of this low-dissipation characteristic and because operation in a complementary mode is highly tolerant of MOSFET electrical parameters, CMOS circuits are suitable for large arrays.

Integrated CMOS arrays are very well suited to logic applications. A wide range of complex functions, such as counters, memories, shift registers and random logic having excellent electrical characteristics and stability up to +125°C ambients, are feasible today. The CMOS arrays offer microwatt power quiescent operation, fast clock rates, and excellent noise immunity. In addition one power supply operation is obtained over a wide range of voltages; in some applications as low as 3 volts. This compares favorably to power requirements of P-channel or N-channel devices, which require 12 volts and more.

CMOS units are capable of interfacing with bipolar logic as do all our MOS devices. High yields are attainable because CMOS logic gates are relatively independent of the electrical characteristics of the individual MOS device.

Methods for the design of CMOS logic can differ and the method ultimately chosen depends on the designer and his particular application:

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1. Direct functional design
2. Gate design
3. Design from "truth tables"

Method 1 is best suited for functional circuits such as shift registers, and counters. Methods 2 and 3 are best suited for circuits in which logic information is easily written with use of mathematical formulas, such as random logic and memories.

On some occasions, it is not unusual to use both methods for making comparisons of equal performance. NOR logic is used whenever possible rather than NAND logic, as this tends to conserve space on the chip.

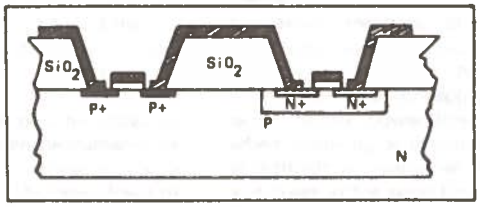


Figure 1: Complementary Metal Oxide Semiconductor (CMOS)

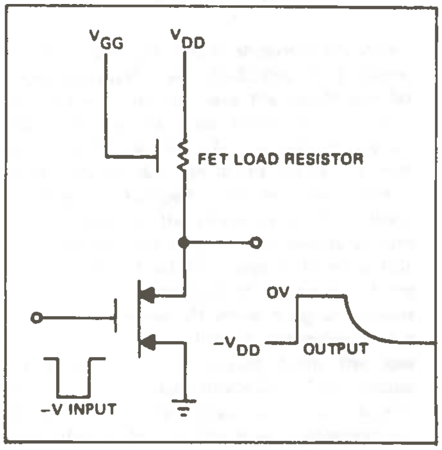


Figure 2: Typical Switching Node, MOSFET Circuit Development.

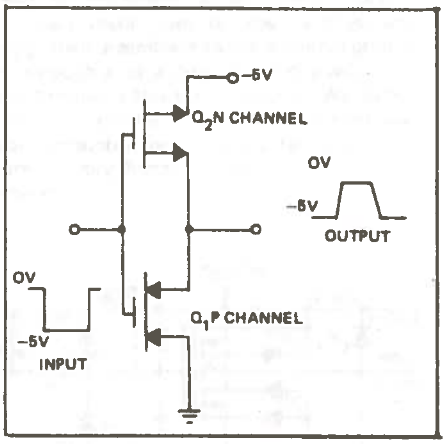


Figure 3: Complementary Switch Using Insulated Gate Field Effect Transistors.

APPENDIX B

CMOS HANDLING CONSIDERATION

TECHNICAL BULLETIN NO. 2

by Irwin Lucks

While we like to think that CMOS devices have a very adequate input protection plan, far better than any single polarity MOS device, nevertheless there is a serious handling and testing problem encountered. Due to the inherently high input impedance on the inputs, a certain amount of care is required to reduce failure of MOS devices during manufacture, testing, shipping, inspection and assembly by equipment manufacturers.

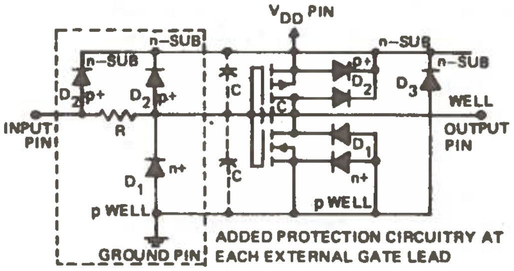
Because input impedance is on the order of 10^{14} ohms, the gate oxide can be damaged or ruptured as a result of only one voltage excursion beyond the breakdown limit. The breakdown of the oxide is approximately 100 volts, however it is not unreasonable to have static charges develop up to many thousands of volts, far more than is necessary to exceed the oxide breakdown. Typically a man's silk tie will measure 2KV static charge, a nylon shirt or smock up to 2KV, a plastic "baggie" can measure up to 4KV.

The diode protection circuit shown in the drawing, is incorporated in all CMOS circuits to eliminate the static build up, and the result is a far better scheme than the single diode used on single polarity MOS, P-Channel or N-Channel. However, it cannot prevent damage at all times if a high static charge is "dumped" into an input. Additionally, because of the presence of this diode protection circuit, the V_{DD} power supply should not be turned off while a signal from a low impedance source is applied at an input. If the V_{DD} supply is turned off while a signal appears at an input, the V_{DD} line is grounded and a positive potential is impressed from the low impedance source, across diode D_2. This voltage if not current limited may cause permanent damage to the diode or to the V_{DD} metallization. Any input excursion above V_{DD} or below V_{SS} should be limited to 50mA for safe operation.

For safety —, the following is recommended:

1. Soldering irons (low voltage preferred) with grounded tips.
2. Reflow soldering or wave soldering equipment grounded to a common point.
3. Do not place units into plastic "baggies", or containers unless it is known that they have been treated with an antistatic chemical.
4. Personnel should not wear rubber-soled shoes, or stand on rubber or plastic mats or wear nylon or plastic gloves while handling a MOS device.
5. When inserting or removing a device, operators should attempt to "short" as many leads as possible with their fingers.
6. Power-up before applying signal and remove signal before power-down. This is important when removing or inserting P. C. Boards since it is difficult to guarantee that all contacts make and break at the same time.
7. All unused inputs should be referenced to either V_{SS} or V_{DD} (dependent on whether its a NOR or NAND function). Never allow an input to "float".

The recommendations given in items 1 through 7 are easy to implement, some manufacturers include sheet metal tops on the benches, and "wiring" their assemblers to the common ground point through a metal bracelet on one wrist connected through a flexible conductor. We do not recommend the latter however, unless the bracelet and/or conductor incorporate a fast breakaway feature, — very handy in case of fire or other emergency.



ADDED PROTECTION CIRCUITRY AT EACH EXTERNAL GATE LEAD

DIODE BREAKDOWNS

D_1 = n^+ TO p WELL 25V MAX

D_2 = p^+ TO n SUB 50V

D_3 = n SUB TO p WELL 100V

R = NORMAL p^+ DIFFUSION IN n SUB ISOLATION

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RECOMMENDED MOS PRECAUTIONS

SUMMARY

Solitron has designed into its MOS Integrated Circuits an effective input protection circuit. However, any MOS circuit can be catastrophically damaged by excessive electrostatic discharge or transient voltages. The following procedures are recommended for those who wish to take full precaution to avoid accidental circuit damage.

Testing MOS Circuits:

1. All units should be tested in plastic carriers. This precludes accidental touching of individual leads.
2. If units are to be tested without carriers, the following precautions should be taken:
    a) A conductive plastic table top should be tied electrically to the test equipment and to the operator (a grounding bracelet is recommended). The common potential should be building ground.
    b) The units are best transported in the plastic antistatic shipping tubes or metal trays.

Test Equipment (Including environmental equipment):

1. All equipment must be properly returned to the same reference (ground) potential as the devices, the operator, and the container for the device.
2. Be especially careful of high voltage surges developed by:
    a) Turning electrical equipment on or off.
    b) Relays
    c) Transients from voltage sources (AC line or power supplies).

Assembly MOS Devices Onto P.C. Boards:

1. The MOS circuits should be mounted on the P.C. board last.
2. Similar precautions should be taken as in Item 2 above at the assembly work station.
3. Soldering irons or solder baths should be at the same reference (ground) potential as the devices.

Package Handling:

1. Precaution must be taken not to subject the package to excessive voltage (i.e., static charge).

General:

1. The handler should take every precaution that the devices will see the same reference potential when they are moving from one point to another.
2. Anyone handling individual devices should develop a habit of first touching the container in which the units are stored before touching the units.
3. Before placing the units into a P.C. board, the handler should touch the P.C. board first.
4. If the MOS devices are to be transferred from one container to another, touch both containers before transferring.
5. Personnel should not wear clothing which will build up static charges. They should wear smocks and clothing made of cotton rather than wool or synthetic fibers.
6. Be careful of electrostatic build up through the movement of air over plastic material. This is especially true of acid sinks.

APPENDIX C

3-1/2 DIGIT COUNTER DISPLAY DEVICE

CM4102

PRELIMINARY DATA SHEET

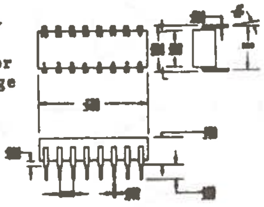
The CM4102 is very low power complementary MOS/LSI universal 3-1/2 decade counter with BCD data storage and drivers. The CM4102 is ideal for DVM, DPM, and digital counter applications.

FEATURES

- Very low operating power, 2mW typical
- Inputs are fully protected
- Single supply voltage
- 16 pin DIL packaging
- High noise immunity
- Electrostatic protection provided on all terminals.

PACKAGING

Lead frame may
be attached to
either the side or
bottom of package



Suffix Definitions

"A" = 3 – 7 [redacted] volt operation
"D" = Hermetic Dual-in-line packaging
"E" = Epoxy Dual-in-line packaging
ALTERNATE PACKAGING AVAILABLE AT
CUSTOMER REQUEST

Maximum Ratings

Operating Voltage (V_{DD}-V_{SS})	3 to 7 [redacted] volts
DC Supply Voltage	–0.5 to + 7 [redacted] volts
All Inputs	$V_{SS} \leq V_{IN} \leq V_{DD}$
Operating Temperature "D"	–55° to +125°C
"E"	–40° to +85°C
Storage Temperature	–65° to +150°C
Power Dissipation	200 milliwatts

TERMINAL CONNECTIONS

1 = O1
2 = O2
3 = Clock Input
4 = Data State
5 = Reset
6 = MUX Input
7 = DD1
8 = V_{SS}

9 = DD2
10 = DD3
11 = DD4
12 = BCD-1
13 = BCD-2
14 = BCD-4
15 = BCD-8
16 = V_{DD}

ELECTRICAL CHARACTERISTICS @25°C (UNLESS OTHERWISE NOTED).

Conditions: $V_{SS} = 0$ V, $V_{DD} = +5$ V $\pm 10\%$

	Level	Minimum	Maximum	Units
All input logic levels	"0" "1"	V_{SS} V_{DD}-1.0	V_{SS} +1.0 V_{DD}	Volts
Digit driver outputs with 1 TTL Load	"0" "1"	V_{SS} V_{DD}-1.0	V_{SS} +.5	Volts
BCD outputs with 1 TTL Load	"0" "1"	V_{SS} V_{DD}-1.0	V_{SS} +.5	Volts
Clock outputs with 1 TTL Load	"0" "1"	V_{SS} V_{DD}-1.0	V_{SS} +.5	Volts

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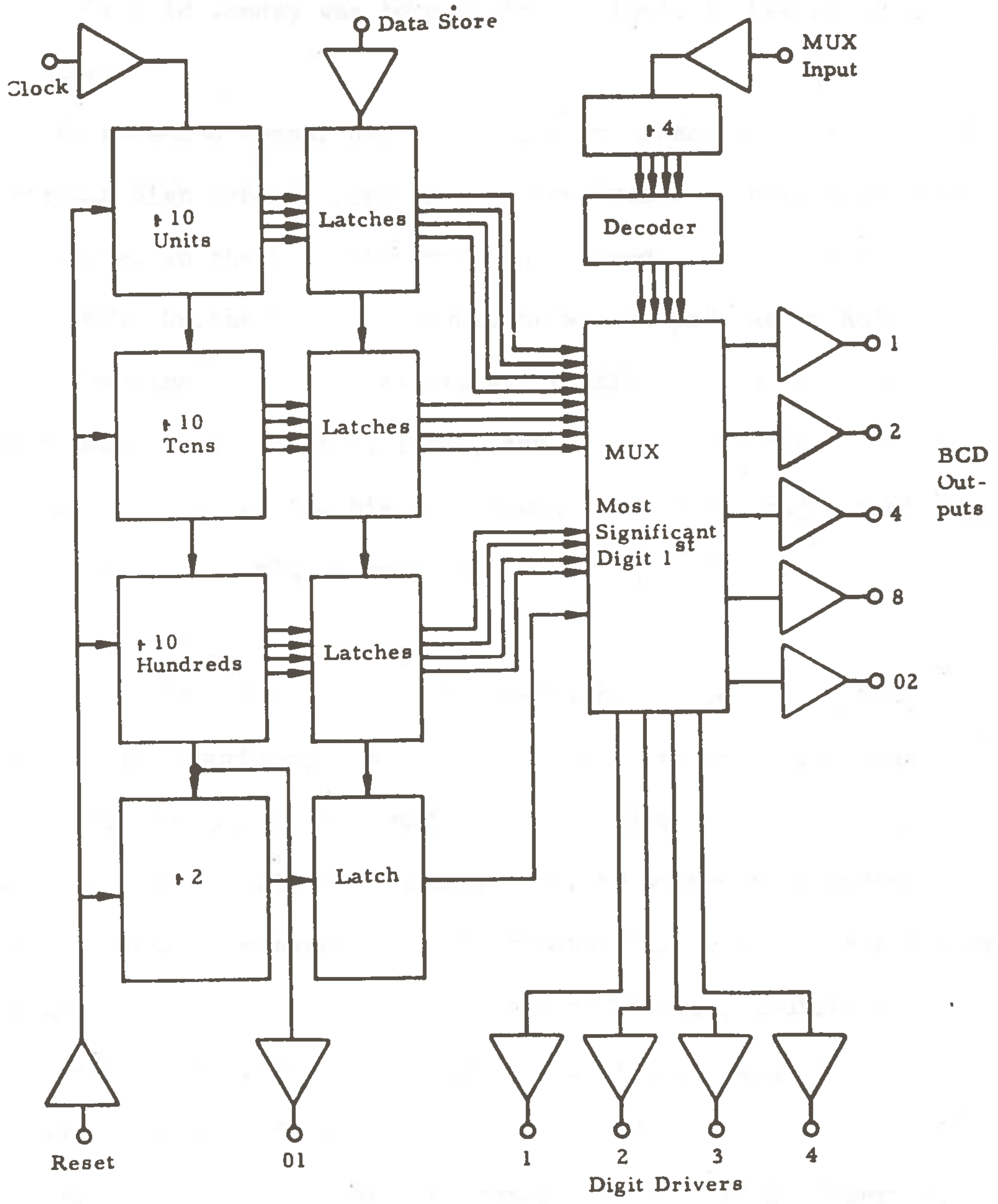

3-1/2 Digit BCD Counter

VITA

John Reid Landry was born on May 6, 1945, in New Orleans, Louisiana.

He attended Kenner High School, Norco Elementary School, and Destrehan High School. Upon graduation from Destrehan High School, he enlisted in the U.S. Air Force and served from June 1963 to June 1967. During his enlistment, he was trained as an Automatic Tracking Radar Specialist, was stationed at a number of Radar Bomb Scoring installations, and achieved the final rank of E-4 (Sergeant). During his enlistment, he had two major modifications to the AN/MSQ-39 radar sytem put into effect throughout the Air Force.

Upon completion of his enlistment, he worked as a computer field engineer and radar technician prior to entering Louisiana State University. After obtaining a Bachelor of Science in Business Administration in August 1971, he worked as a radio station manager, manager of a distributor for standby power systems, and as an Associate in the Department of Physics, Louisiana State University. He entered graduate school of Louisiana State University in August 1973.

He is a candidate for the degree of Master of Engineering, majoring in Nuclear Engineering and a Business minor.

EXAMINATION AND THESIS REPORT

Candidate: John Reid Landry

Major Field: Nuclear Engineering

Title of Thesis: The Design and Evaluation of a Preset, Alarming, Electronic Dosimeter

Approved:

Frank A. Iddings
Major Professor and Chairman

Dean of the Graduate School

EXAMINING COMMITTEE:

Edmund R. Gray

John C Courtney

Date of Examination:

April 18, 1975